E R A

Embedded Reconfigurable Architectures

ERA aims at investigating and developing new methodologies in both tools and hardware designs to break through current power and memory walls and help design the next-generation embedded systems platforms. The proposed strategy is to utilize adaptive hardware to provide the highest possible performance with limited power budgets. The envisioned ERA platform is adaptive and employs a structured design to integrate the necessary computing, networking, and memory elements.

At A Glance: ERA

Embedded Reconfigurable Architectures

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reconfigurable/adaptive computing, memory hierarchies, power models, parameterized processor designs, dynamic reconfiguration, power awareness, structured embedded systems design, application profiling and benchmarking, embedded Linux, reconfiguration-aware compilation algorithms, fault-tolerance, dynamic parallel execution, gcc compiler.

Main Objectives

In the Objective ICT-2009.3.4 "Embedded Systems Design", a strong focus is placed on the development of novel (generic) design methodologies that can be applied to several application areas. In the ERA project, we describe a platform that can adapt itself through coarse-grain reconfigurable hardware to tailor the hardware itself for changing environments and needs of the applications running on the platform, for different application markets and platform usage. We identified the following main objectives:

ERA will focus on the development of an adaptive embedded systems platform to handle the challenges of current embedded processor designs

- to define and develop a dynamically reconfigurable integrated platform composed by the following components: a parameterized VLIW processor, a reconfigurable NoC, and a memory subsystem - taking into account power consumption as design parameter.
- to provide the support for flexible and fast reconfiguration of the platform by using direct hardware support as well as partial FPGA reconfiguration.
- to provide the needed hardware monitoring and low-level OS support to efficiently control the hardware reconfiguration.
- to benchmark and analyze a set of existing applications in the area of mobile processing to extract a set of off-line and on-line measurable parameters.

- to build a supervisor which will be able to monitor the parameters and react to online application changes to appropriately reconfigure the hardware.

The envisioned **adaptive ERA platform** employs a structured design approach that allows integration of varying computing elements, networking elements, and memory elements. For computing elements, we will utilize a mixture of commercially available off-the-shelf processor cores, industry-owned IP cores, and application-specific/dedicated cores, and we will dynamically adapt their composition, organization, and even instruction-set architectures to provide the best possible performance/power trade-offs. Similarly, the choice of the most-suited network elements and topology and the adaptation of the hierarchy and organization of the memory elements can be determined at design-time or at run-time. Furthermore, the envisioned adaptive platform must be supported by and/or made visible to the application(s), run-time system, operating system, and compiler exploiting the synchronicities between software and hardware. We strongly believe that having the complete freedom to flexibly tune the hardware elements will allow for a much higher level of efficiency (e.g., riding the trade-off curve between performance and power). Finally, an additional goal of the adaptive platform is to serve as a quick prototyping platform in embedded systems design.

Technical Approach

In the ERA project, we identified four key areas to pursue innovations in order to achieve our objectives:

- definition and characterization of application benchmarks for embedded systems employing reconfigurable architectures.
- definition of a reconfigurable and parameterized processor architecture.
- definition of a reconfigurable memory subsystem.
- definition of the software/compiler tools and OS support for the ERA platform.

The applications exhibit behaviour that can be exploited for more efficient processing (at given power budgets) by adapting the hardware (processor and memory) to them. This paradigm shift requires new approaches in compiler algorithms and tools and advanced (embedded) OS-level support. All partners have expertise in one or several of the mentioned areas.

Key Issues

We believe that the run-time adaptive behaviour of the ERA platform is the key to develop embedded platforms for the new, heterogeneous and multi-applications embedded market. A major concern is the power utilization. This translates in several key issues that must be addressed in order to achieve a breakthrough. To cope with the reconfiguration power problem, in this project we focus on the development of **accelerators using a coarse-grain reconfigurable fabric**, composed of a **reconfigurable VLIW processor**, a **flexible memory organization** and an **interconnection network that can provide better usage of power resources** by distributing its routing resources online. A software stack consisting of a **compiler** and **OS** will provide the means to drive both **static and dynamic reconfiguration decisions** according to the application characteristics and the user objectives (in terms of power and performance).

Expected Impact

The industrial partners clearly identified the benefits of the ERA project expressed in their involvement in and commitment to the project. All the solutions proposed in this project will be combined in a demonstrator platform that we expect will allow the industrial partners fast access to new products developed on top of it. The intended platform will serve several purposes:

- ***Quick development platform for the industry:*** the clear interfaces defined in this project should allow the industrial partners to take from the platform everything they need and still incorporate their own IPs. Moreover, for low volumes even the prototype can be used as a commercially viable product, since the consortium will use available FPGA technology to validate its contribution.
- ***Academic purposes:*** the ERA platform can be easily used to build different instances of embedded processing solutions and we foresee and will actively pursue the possibility of incorporating the ERA platform as a teaching tool in embedded courses or labs.