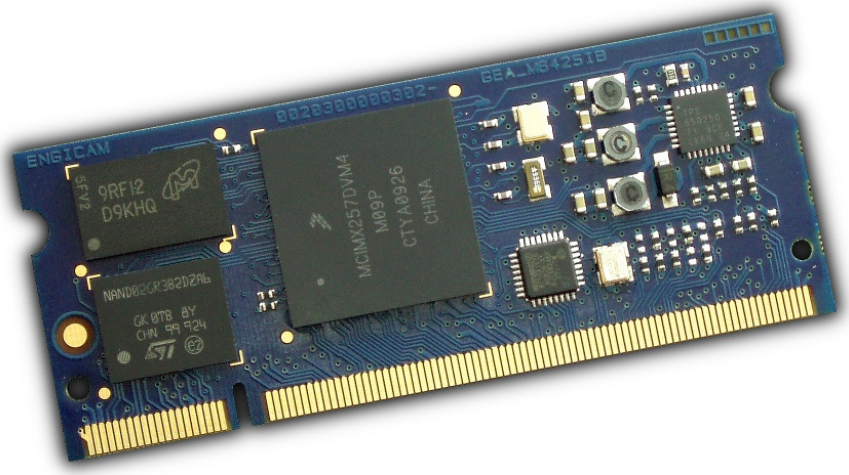
GEA M6425 IB

Getting started manual



***** REV I *****

ATE	REVISION	CHANGE DESCRIPTION
19/05/10	-	Creation
25/05/10	A	Added supply features
08/06/10	B	Modify tables, insert pin number column, change Ethernet description, change figure 9
11/06/10	C	Added Module GEA 's photo, Added signal's description
29/06/10	D	Added periheral multiplexing description chapter, Added power supply considerations
05/07/10	E	Change pin number of table22, added PWM pins, IIC and GPT 's alternative interfaces
20/09/10	F	Added note to application with 3,3V PWR Supply
06/10/10	G	Added note to connectig LCD color's signals interface. Added I.MX25's pin name in the table of Pin Out. Changed SD's figure
19/11/10	H	Added UARTs alternative interfaces; modify SD card interface's chapter
03/12/10	I	Add module connector's type; pin out taable update

Summary

GEA M6425 Mechanical data

The GEA M6425 module has a standard SODIMM footprint. The PCB dimensions is L 67.60 x W 27 x H 1 mm. A picture is shown in the Figure 1.

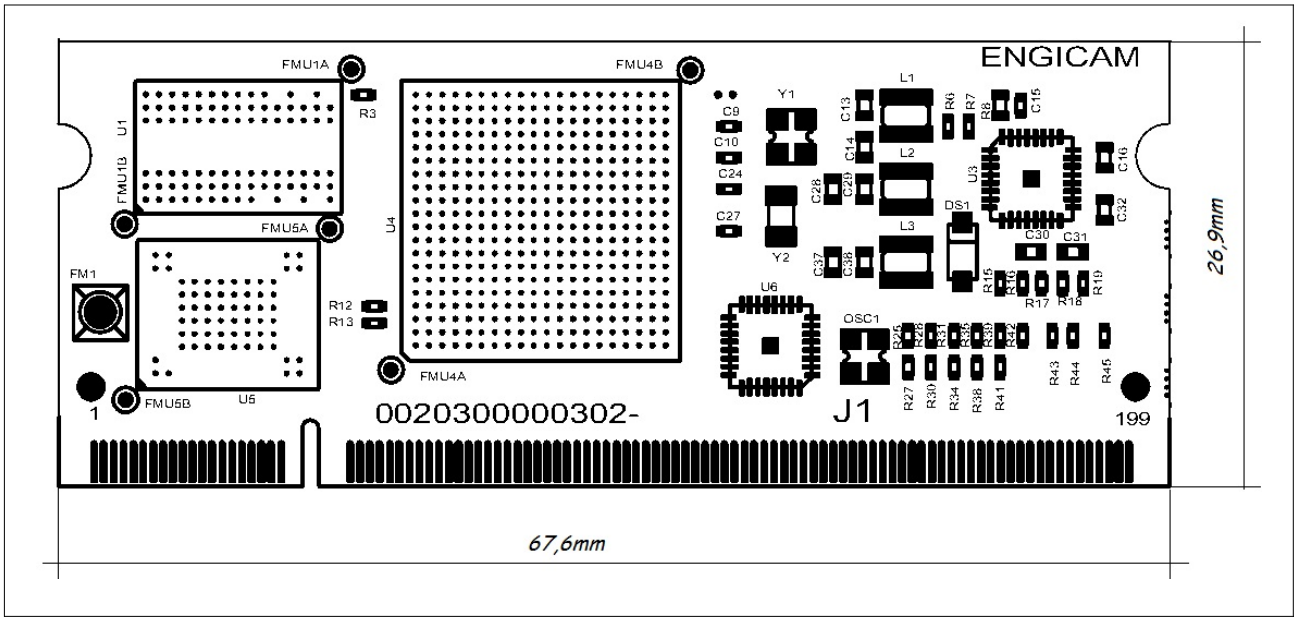


Figure 1

GEA M6425 Pin OUT

The module's interface is achieved by a SO DIMM 200 position connector TYCO ELECTRONICS code 1473005-1 or compatible

Pin	Name	Pin Name on I.MX25	Primary Function Description	GPIO Capable	Voltage
1	+1,8V	-	Output Power PIN	N	-
2	+1,8V	-	Output Power PIN	N	-
3	GND	-	Power PIN	N	-
4	GND	-	Power PIN	N	-
5	GND	-	Power PIN	N	-
6	CSI_D[2]	CSI_D2	CMOS Sensor Interface Data 2	Y	+3,3V
7	CSI_D[3]	CSI_D3	CMOS Sensor Interface Data 3	Y	+3,3V
8	CSI_D[4]	CSI_D4	CMOS Sensor Interface Data 4	Y	+3,3V
9	CSI_D[5]	CSI_D5	CMOS Sensor Interface Data 5	Y	+3,3V
10	CSI_D[6]	CSI_D6	CMOS Sensor Interface Data 6	Y	+3,3V
11	CSI_D[7]	CSI_D7	CMOS Sensor Interface Data 7	Y	+3,3V
12	CSI_D[8]	CSI_D8	CMOS Sensor Interface Data 8	Y	+3,3V
13	CSI_D[9]	CSI_D9	CMOS Sensor Interface Data 9	Y	+3,3V
14	CSI_VSYNC	CSI_VSYNC	CMOS Sensor Interface Vertical Sync	Y	+3,3V
15	CSI_HSYNC	CSI_HSYNC	CMOS Sensor Interface Horizontal Sync	Y	+3,3V
16	CSI_PIXCLK	CSI_PIXCLK	CMOS Sensor Interface Pixel Clock	Y	+3,3V
17	CSI_MCLK	CSI_MCLK	CMOS Sensor Interface Sensor Master Clock	Y	+3,3V
18	NC	-	RFU reserved	-	-
19	NC	-	RFU reserved	-	-
20	NC	-	RFU reserved	-	-
21	NC	-	RFU reserved	-	-
22	GND	-	Power PIN	N	-
23	I2C1_SCL	I2C1_CLK	I2C SCL Signal	Y	+3,3V
24	I2C1_SDA	I2C1_DAT	I2C SDA Signal	Y	+3,3V
25	TOUCH_XP	XP	Touch Screen Xp	N	+3,3V
26	TOUCH_XN	XN	Touch Screen Xn	N	+3,3V
27	TOUCH_YP	YP	Touch Screen Yp	N	+3,3V
28	TOUCH_YN	YN	Touch Screen Yn	N	+3,3V
29	ADC_1	INAUX0	ADC input 1	N	+3,3V
30	ADC_2	INAUX1	ADC input 2	N	+3,3V
31	GND	-	Power PIN	N	-
32	ADC_3	INAUX2	ADC input 3	N	+3,3V
33	ADC_4	WIPER	ADC input 4	N	+3,3V
34	MISC_GPIO01	EXT_ARMCLK	Generic GPIO (3,3V)	Y	+3,3V
35	MISC_GPIO02	UPLL_BYPCLK	Generic GPIO (3,3V)	Y	+3,3V
36	MISC_GPIO03	VSTBY_REQ	Generic GPIO (3,3V)	Y	+3,3V
37	MISC_GPIO04	VSTBY_ACK	Generic GPIO (3,3V)	Y	+3,3V
38	MISC_GPIO05	POWER_FAIL	Generic GPIO (3,3V)	Y	+3,3V
39	NC	-	NC	-	-
40	MISC_GPIO07	CLKO	Generic GPIO (3,3V)	Y	+3,3V
41	NC	-	Ethernet 2 reserved	-	-
42	NC	-	Ethernet 2 reserved	-	-
43	NC	-	Ethernet 2 reserved	-	-
44	NC	-	Ethernet 2 reserved	-	-
45	NC	-	Ethernet 2 reserved	-	-
46	NC	-	Ethernet 2 reserved	-	-
47	NC	-	Ethernet 2 reserved	-	-
48	NC	-	GPIO 3V3 reserved	-	-
49	NC	-	GPIO 3V3 reserved	-	-
50	NC	-	GPIO 3V3 reserved	-	-

Pin	Name	Pin Name on I.MX25	Primary Function Description	GPIO Capable	Voltage
51	NC	-	DAC reserved	-	-
52	NC	-	DAC reserved	-	-
53	Bus_A20	A20	Bus Expansion Pin	Y	+1,8V
54	Bus_A17	A17	Bus Expansion Pin	Y	+1,8V
55	BUS_EB1	EB1	Bus Expansion Pin	Y	+1,8V
56	BUS_A21	A21	Bus Expansion Pin	Y	+1,8V
57	BUS_RW	RW	Bus Expansion Pin	Y	+1,8V
58	BUS_A16	A16	Bus Expansion Pin	Y	+1,8V
59	BUS_CS0	CS0	Bus Expansion Pin	Y	+1,8V
60	BUS_CS5_DTACK	CS5	Bus Expansion Pin	Y	+1,8V
61	BUS_CS2	CS4	Bus Expansion Pin	Y	+1,8V
62	BUS_CS1	CS1	Bus Expansion Pin	Y	+1,8V
63	BUS_A19	A19	Bus Expansion Pin	Y	+1,8V
64	GND	-	Power PIN	N	-
65	BUS_EB0	EB0	Bus Expansion Pin	Y	+1,8V
66	BUS_BCLK	BCLK	Bus Expansion Pin	Y	+1,8V
67	BUS_WAIT	ECB	Bus Expansion Pin	Y	+1,8V
68	BUS_A18	A18	Bus Expansion Pin	Y	+1,8V
69	BUS_LBA	LBA	Bus Expansion Pin	Y	+1,8V
70	BUS_OE	OE	Bus Expansion Pin	Y	+1,8V
71	GND	-	Power PIN	N	-
72	NC	-	RFU reserved	-	-
73	AD9	D9	Bus Expansion Pin	Y	+1,8V
74	NC	-	RFU reserved	-	-
75	AD0	D0	Bus Expansion Pin	Y	+1,8V
76	NC	-	RFU reserved	-	-
77	AD2	D2	Bus Expansion Pin	Y	+1,8V
78	NC	-	RFU reserved	-	-
79	AD8	D8	Bus Expansion Pin	Y	+1,8V
80	AD1	D1	Bus Expansion Pin	Y	+1,8V
81	AD11/'USB_OTG_PWR_EN'	D11	Bus Expansion Pin	Y	+1,8V
82	AD3	D3	Bus Expansion Pin	Y	+1,8V
83	AD10/'USB_OTG_OC'	D10	Bus Expansion Pin	Y	+1,8V
84	AD12	D12	Bus Expansion Pin	Y	+1,8V
85	AD5	D5	Bus Expansion Pin	Y	+1,8V
86	AD7	D7	Bus Expansion Pin	Y	+1,8V
87	AD4	D4	Bus Expansion Pin	Y	+1,8V
88	NC	-	RFU reserved	-	-
89	GND	-	Power PIN	N	-
90	NC	-	RFU reserved	-	-
91	AD6	D6	Bus Expansion Pin	Y	+1,8V
92	MISC_GPIO06	CSPI1_RDY	Generic GPIO (3,3V)	Y	+3,3V
93	AD13	D13	Bus Expansion Pin	Y	+1,8V
94	PWM_OUT	PWM	PWM Out signal	Y	+1,8V
95	AD14	D14	Bus Expansion Pin	Y	+1,8V
96	NC	-	PWM2 reserved	-	-
97	AD15	D15	Bus Expansion Pin	Y	+1,8V
98	NC	-	RFU reserved	-	-
99	NC	-	RFU reserved	-	-
100	NC	-	RFU reserved	-	-

Pin	Name	Pin Name on I.MX25	Primary Function Description	GPIO Capable	Voltage
101	'UART4_CTS'	KPP_COL3	UART4 CTS signal	Y	+3,3V
102	UART4_RTS	KPP_COL2	UART4 RTS signal	Y	+3,3V
103	UART4_TXD	KPP_COL1	UART4 TXD signal	Y	+3,3V
104	UART4_RXD	KPP_COL0	UART4 RXD signal	Y	+3,3V
105	UART3_CTS	KPP_ROW3	UART3 CTS signal	Y	+3,3V
106	UART3_RTS	KPP_ROW2	UART3 RTS signal	Y	+3,3V
107	GND	-	Power PIN	N	-
108	UART3_TXD	KPP_ROW1	UART3 TXD signal	Y	+3,3V
109	UART3_RXD	KPP_ROW0	UART3 RXD signal	Y	+3,3V
110	UART2_CTS	UART2_CTS	UART2 CTS signal	Y	+3,3V
111	UART2_RTS	UART2_RTS	UART2 RTS signal	Y	+3,3V
112	UART2_TXD	UART2_TXD	UART2 TXD signal	Y	+3,3V
113	UART2_RXD	UART2_RXD	UART2 RXD signal	Y	+3,3V
114	UART1_CTS	UART1_CTS	UART1 CTS signal	Y	+3,3V
115	UART1_RTS	UART1_RTS	UART1 RTS signal	Y	+3,3V
116	UART1_TXD	UART1_TXD	UART1 TXD signal	Y	+3,3V
117	UART1_RXD	UART1_RXD	UART1 RXD signal	Y	+3,3V
118	CAN1_TX/'USB_OTG_PWR_EN'	GPIO_A	CAN 1 transmit signal / USB on the go interface	Y	+3,3V
119	CAN1_RX/'USB_OTG_OC'	GPIO_B	CAN 1 receive signal / USB on the go interface	Y	+3,3V
120	CAN2_TX	GPIO_C	CAN 2 transmit signal	Y	+3,3V
121	CAN2_RX	GPIO_D	CAN 2 receive signal	Y	+3,3V
122	NC	-	RFU reserved	-	-
123	GND	-	Power PIN	N	-
124	NC	-	RFU reserved	-	-
125	LCD_LSCLK_PCLK_FPSHIFT	LSCLK	LCD interface	Y	+3,3V
126	NC	-	LCD reserved	-	-
127	ETH_TXN	-	Fast Ethernet Controller TXN signal	-	+3,3V
128	NC	-	LCD reserved	-	-
129	ETH_TXP	-	Fast Ethernet Controller TXP signal	-	+3,3V
130	NC	-	LCD reserved	-	-
131	ETH_RXN	-	Fast Ethernet Controller RXN signal	-	+3,3V
132	LCD_CONTRAST	CONTRAST	LCD interface	N	+3,3V
133	ETH_RXP	-	Fast Ethernet Controller RXP signal	-	+3,3V
134	+3V3	-	Output Power PIN	N	-
135	+3V3	-	Output Power PIN	N	-
136	NC	-	LCD reserved	-	-
137	ETH_LED_10_100_KATHOD	-	Led Indicator Kathod signal	Y	+3,3V
138	NC	-	LCD reserved	-	-
139	ETH_LED_ACT_ANOD	-	Led indicator Anod signal	Y	+3,3V
140	NC	-	LCD reserved	-	-
141	LCD_D17	GPIO_F	LCD interface	Y	+3,3V
142	LCD_D16	GPIO_E	LCD interface	Y	+3,3V
143	LCD_D15	LD15	LCD interface	N	+3,3V
144	LCD_D14	LD14	LCD interface	N	+3,3V
145	LCD_D13	LD13	LCD interface	N	+3,3V
146	LCD_D12	LD12	LCD interface	N	+3,3V
147	LCD_D11	LD11	LCD interface	N	+3,3V
148	LCD_D10	LD10	LCD interface	N	+3,3V
149	LCD_D9	LD9	LCD interface	N	+3,3V
150	LCD_D8	LD8	LCD interface	N	+3,3V

Pin	Name	Pin Name on I.MX25	Primary Function Description	GPIO Capable	Voltage
151	LCD_D7	LD7	LCD interface	Y	+3,3V
152	LCD_D6	LD6	LCD interface	Y	+3,3V
153	LCD_D5	LD5	LCD interface	Y	+3,3V
154	LCD_D4	LD4	LCD interface	Y	+3,3V
155	LCD_D3	LD3	LCD interface	Y	+3,3V
156	GND	-	Power PIN	N	-
157	LCD_D2	LD2	LCD interface	Y	+3,3V
158	LCD_D1	LD1	LCD interface	Y	+3,3V
159	LCD_D0	LD0	LCD interface	Y	+3,3V
160	LCD_VSYNC	VSYNC	LCD interface	Y	+3,3V
161	LCD_HSYNC	HSYNC	LCD interface	Y	+3,3V
162	LCD_OE	OE_ACD	LCD interface	Y	+3,3V
163	NC	-	SPI2 reserved	-	-
164	NC	-	SPI2 reserved	-	-
165	NC	-	SPI2 reserved	-	-
166	NC	-	SPI2 reserved	-	-
167	CSPI_MOSI/UART3_RXD	CSPI1_MOSI	CSPI MOSI	Y	+3,3V
168	CSPI_MISO/UART3_TXD	CSPI1_MISO	CSPI MISO	Y	+3,3V
169	CSPI_CLK	CSPI1_SCLK	CSPI CLK	Y	+3,3V
170	CSPI_SS1/UART3_RTS	CSPI1_SS1	CSPI_SS1	Y	+3,3V
171	CSPI_SS0	CSPI1_SS0	CSPI SS0	Y	+3,3V
172	JTAG_DE	DE_B	JTAG Interface	Y	+3,3V
173	JTAG_TRTS	TRTS	JTAG Interface	N	+3,3V
174	JTAG_TD0	TD0	JTAG Interface	N	+3,3V
175	JTAG_TDI	TDI	JTAG Interface	N	+3,3V
176	JTAG_TMS	TMS	JTAG Interface	N	+3,3V
177	JTAG_TCK	TCK	JTAG Interface	N	+3,3V
178	JTAG_RTCK	RTCK	JTAG Interface	Y	+3,3V
179	'JTAG_RESET'/'MASTER_RESET'	RESET_B	JTAG Interface with Pull-up on module	N	+3,3V
180	NC	-	-	-	-
181	BOOT_MODE	BOOT_MODE0	Boot from USB/Uart or on board Nand Flash	Y	+3,3V
182	GND	-	Power PIN	N	-
183	'SD1_CD'	A15	eSDHC CD Signal	Y	+1,8V
184	'SD1_WP'	A14	eSDHC WP Signal	Y	+1,8V
185	SD1_DAT2	SD1_DATA2	eSDHC DAT 2 signal	Y	+3,3V
186	SD1_DAT3	SD1_DATA3	eSDHC DAT 3 signal	Y	+3,3V
187	SD1_DAT1	SD1_DATA1	eSDHC DAT 1 signal	Y	+3,3V
188	SD1_DAT0	SD1_DATA0	eSDHC DAT 0 signal	Y	+3,3V
189	SD1_CLK	SD1_CLK	eSDHC CLK signal	Y	+3,3V
190	SD1_CMD	SD1_CMD	eSDHC CMD signal	Y	+3,3V
191	USB_OTG_UID	USBPHY1_UID	USB on the go interface	N	+3,3V
192	USB_OTG_DP	USBPHY1_DP	USB on the go interface	N	+3,3V
193	USB_OTG_DM	USBPHY1_DM	USB on the go interface	N	+3,3V
194	USB_FS_DP	USBPHY2_DP	USB HOST interface	N	+3,3V
195	USB_OTG_5V_VBUS	USBPHY1_VBUS	USB on the go interface	N	+3,3V
196	USB_FS_DM	USBPHY2_DM	USB HOST interface	N	+3,3V
197	3V6_IN	-	Power PIN	N	-
198	3V6_IN	-	Power PIN	N	-
199	3V6_IN	-	Power PIN	N	-
200	3V6_IN	-	Power PIN	N	-

Table 1

Assembly Top View

The GEA M6425 has a Standard SODIMM footprint where odd pins are on top (component) side and even pins are on bottom side. In Figure 2 and 3 is shown pin1 and pin 2 positions.

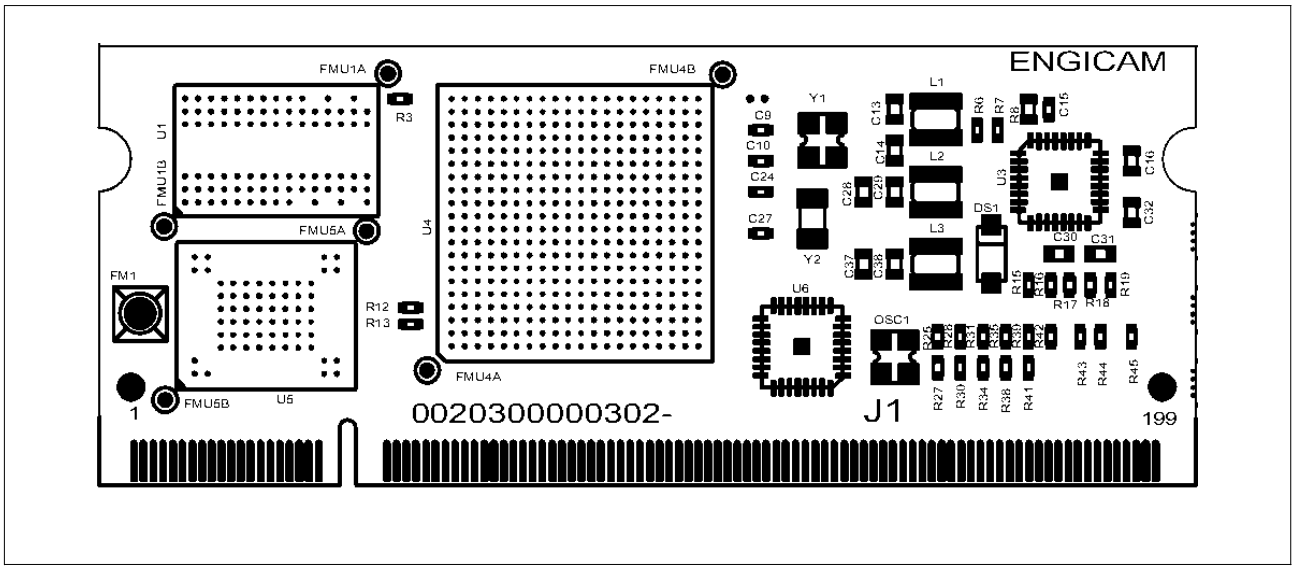


Figure 2

Assembly Bottom View

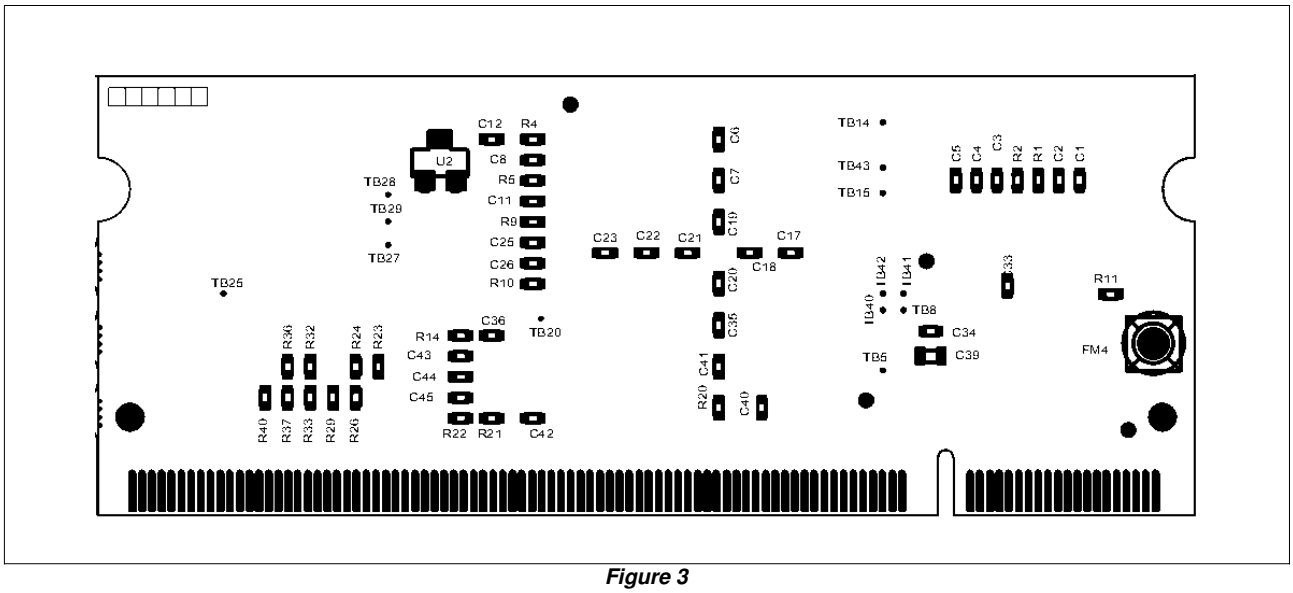


Figure 3

How to power the GEA M6425 module.

GEA M6425 needs only a 3.6V power supply. Please refer to to table 2 for the power supply range specification.

	Min	Typ	Max
Voltage 3V6_IN range	+3,3 V	.	+6,0V
Current @ 3,6V		170 mA	
Current @ 5,0V		130 mA	

Table 2

Notes for applications with +3,3V power supply

There are some considerations to do when we apply a power supply of +3,3V to GEA module. In this case we 've the following measures based on load applied

Voltage supply	Current consumption at +3,3V Output	Voltage drop measured
+3,3V	0 A	20 mV
+3,3V	0,5 A	180-200 mV
+3,3V	0,25 A	90-100 mV

Table 3

Based on the previous measures we suggest the following configurations for the circuit according to current consumption:

1) If main circuit's current consumption is lower than 0,25A we could use the GEA's 3,3V output to power the main board

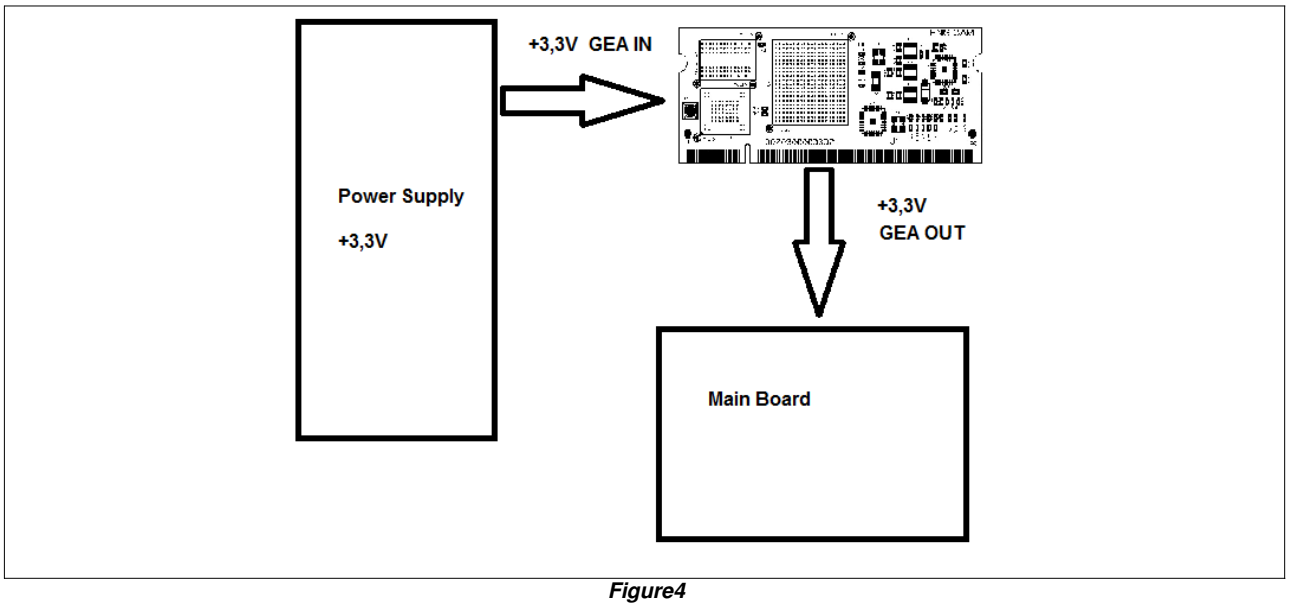


Figure4

2) If main circuit's current consumption is in range 0,25 – 05 A or more, we could use the GEA's +3,3V output to power the main board only if the chips on board are compliant with losses shown in the Table 3 . Otherwise it's better to power the main board directly from the main power (see figure 5 below)

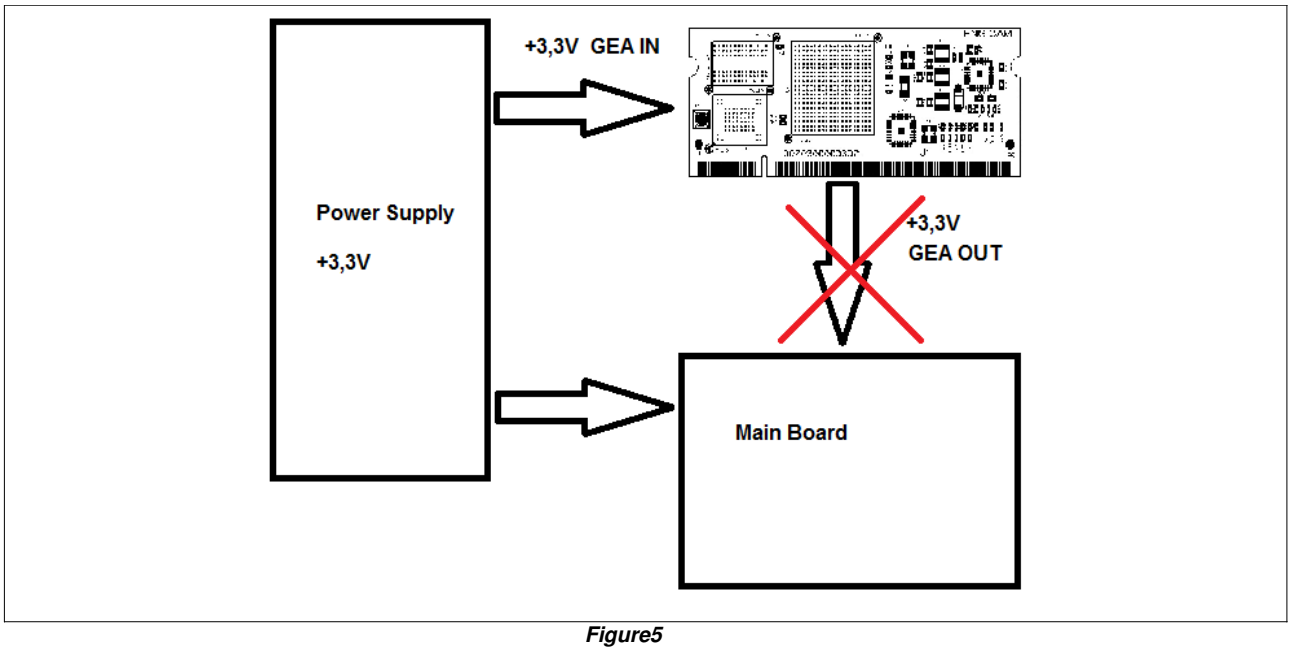


Figure5

In table 4 are shown the GEA M6425 power supply pins numbering, please connect all power supply pins in order to avoid damage.

Number	Name	Primary Function Description	GPIO Capable	Voltage
197	3V6_IN	Power PIN	N	-
198	3V6_IN	Power PIN	N	-
199	3V6_IN	Power PIN	N	-
200	3V6_IN	Power PIN	N	-
3	GND	Power PIN	N	-
4	GND	Power PIN	N	-
5	GND	Power PIN	N	-
22	GND	Power PIN	N	-
31	GND	Power PIN	N	-
64	GND	Power PIN	N	-
71	GND	Power PIN	N	-
89	GND	Power PIN	N	-
107	GND	Power PIN	N	-
123	GND	Power PIN	N	-
156	GND	Power PIN	N	-
182	GND	Power PIN	N	-

Table 4

In the figure 6 is shown the GEA's Started KIT power supply design. Anyway some GEA's peripherals needs an extra power source. Please read carefully the related sections before start your power stage design.

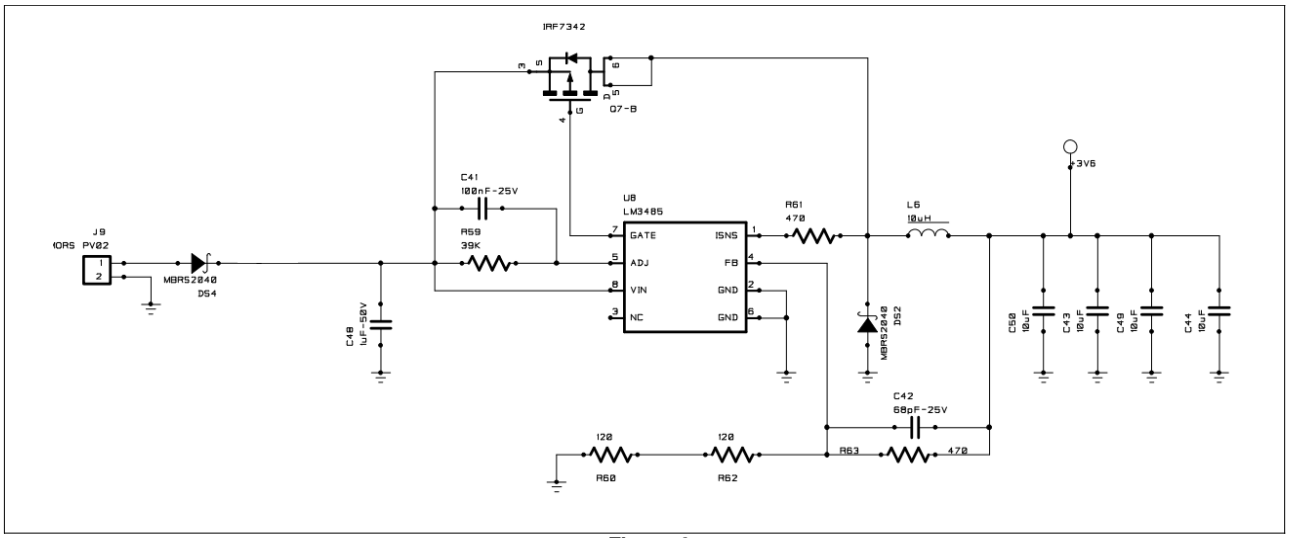


Figure 6

GEA M6425 module has 4 Output power PIN usable for power source. In table 4 are shown the GEA M6425 power supply pins numbering.

Number	Name	Primary Function Description	GPIO Capable	Voltage
134	+3V3	Output Power PIN	N	-
135	+3V3	Output Power PIN	N	-
1	+1V8	Output Power PIN	N	-
2	+1V8	Output Power PIN	N	-

Table 5

In table 6 are shown the maximun rating of power output:

Power output	Max output current
3,3 V outputs	500 mA (Total)
1,8 V outputs	500 mA (Total)

Table 6

How to connect two 3-wire RS232 serial port

In this section is shown how to use the GEA UART1 and UART2 as 3-wire RS232 serial ports.
In table 7 are shown the GEA M6425 UART1 and UART2 pins numbering.

Number	Name	Primary Function Description	GPIO Capable	Voltage
110	UART2_CTS	UART2 CTS signal	Y	+3,3V
111	UART2_RTS	UART2 RTS signal	Y	+3,3V
112	UART2_TXD	UART2 TXD signal	Y	+3,3V
113	UART2_RXD	UART2 RXD signal	Y	+3,3V
114	UART1_CTS	UART1 CTS signal	Y	+3,3V
115	UART1_RTS	UART1 RTS signal	Y	+3,3V
116	UART1_TXD	UART1 TXD signal	Y	+3,3V
117	UART1_RXD	UART1 RXD signal	Y	+3,3V

Table 7

The signal on the GEA UART pins are 3.3V logic level, this can not be connected directly to a RS232 device like a a PC Serial port, the use of a transceivers on the base board is mandatory in order to avoid GEA module damage.

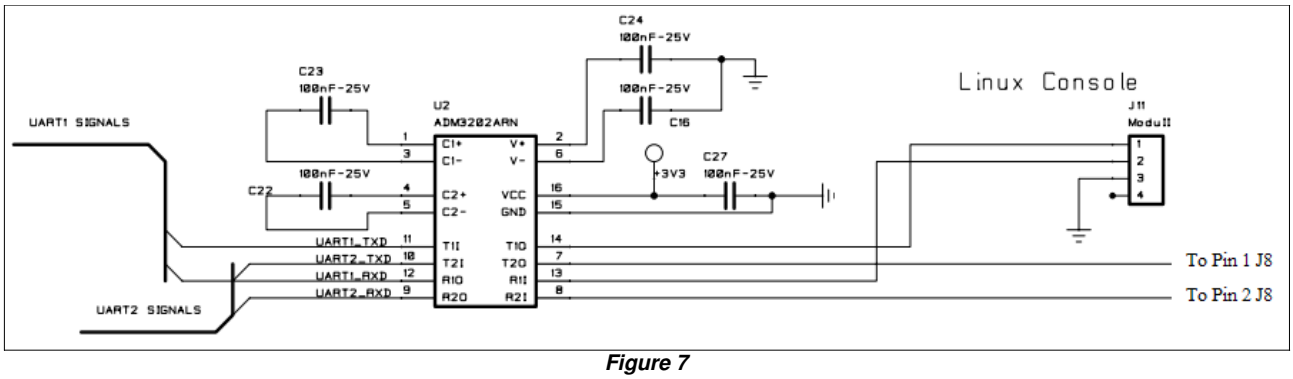


Figure 7

In figure 7 is shown how UART1 and UART2 are connected on the GEA started kit. In this example an ADM3202ARN IC from Analog Device is used like transceiver for both UART without any control signal. In case RTS and CTS are need, a transceiver must be used for this signals.

When Linux is installed on a GEA module, UART1 is used like console. The default communications settings is shown in table 8.

Linux console default settings	
Baud rate	115200
Data length	8 bit
Parity	none
Stop	1bit

Table 8

How to connect a RS485 serial port

In this chapter is shown how an RS485 serial port can be connected to a GEA module. In figure 8 is shown how UART3 is used to connect to a RS485 transceiver on the GEA starter kit. In this case UART3 is used but please consider that any UART ports can be used to connect a RS485 transceiver.

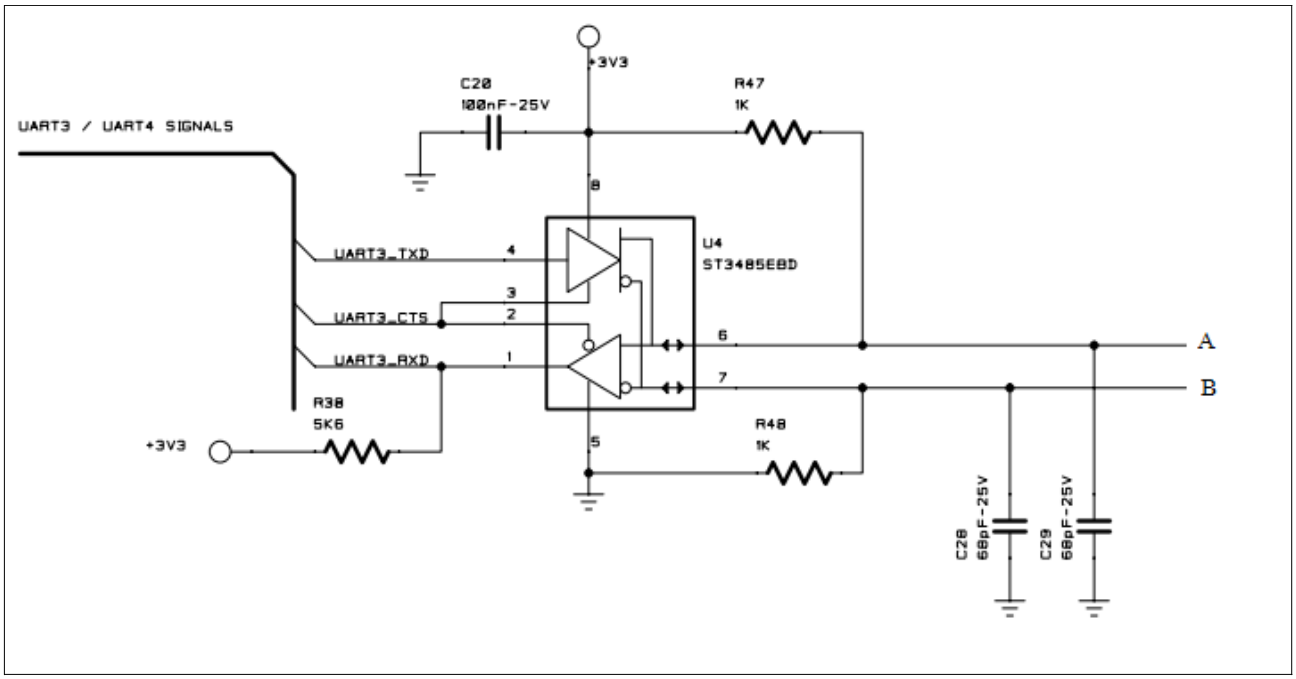


Figure 8

The pins involved in this RS485 communication example are listed in table 9.

Number	Name	Primary Function Description	GPIO Capable	Voltage
105	UART3_CTS	UART3 CTS signal	Y	+3,3V
108	UART3_TXD	UART3 TXD signal	Y	+3,3V
109	UART3_RXD	UART3 RXD signal	Y	+3,3V

Table 9

How to connect a CAN interface

In this chapter is descriped how a CAN bus transceiver can be connected to a GEA module. In figure 9 is shown how CAN is connected on the GEA starter kit where only CAN2 is used, so CAN_TX can be referred to CAN2_TX and CAN_RX to CAN2_RX. If a second CAN ports is needed, CAN1 port can be used in the same way. In Table 10 are listed all CAN signal of GEA module.

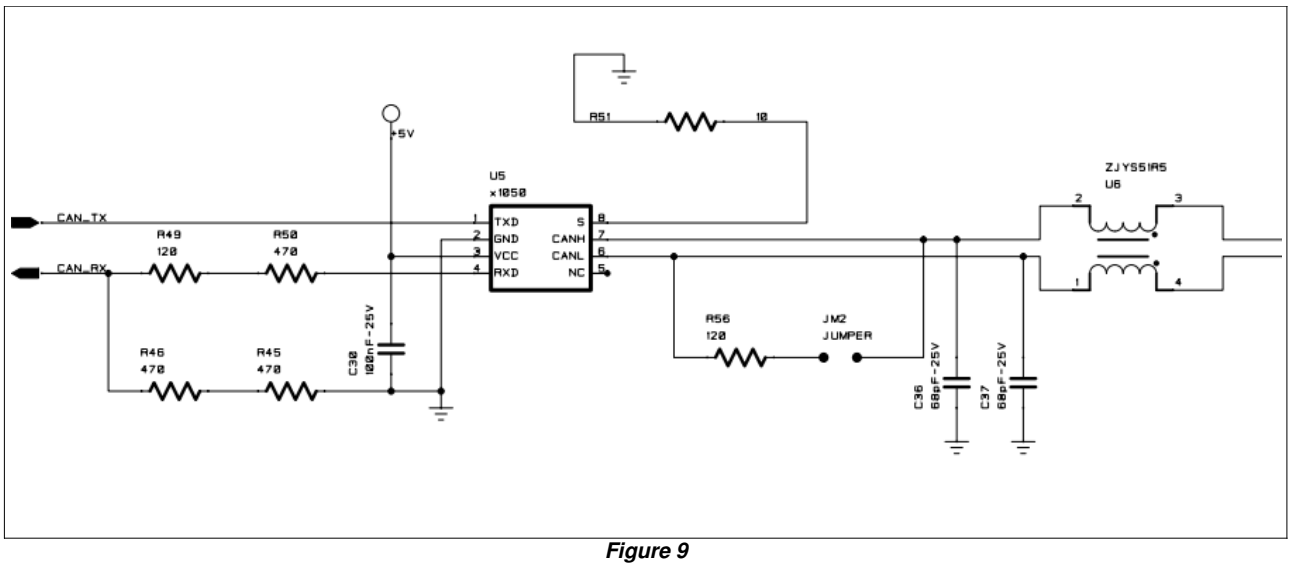


Figure 9

Number	Name	Primary Function Description	GPIO Capable	Voltage
118	CAN1_TX	CAN 1 transmit signal	Y	+3,3V
119	CAN1_RX	CAN 1 receive signal	Y	+3,3V
120	CAN2_TX	CAN 2 transmit signal	Y	+3,3V
121	CAN2_RX	CAN 2 receive signal	Y	+3,3V

Table 10

How to design the Ethernet interface

The Freescale iMx25 Ethernet Media Access Controller (MAC) is designed to support both 10 and 100 Mbps Ethernet/IEEE standard 802.3™ networks. The 10-Mbps and 100-Mbps RMII Ethernet physical interfaces is supported. In figure 10 is shown how to connect the Ethernet interface to GEA module. In table 11 are listed all Ethernet signal of GEA module:

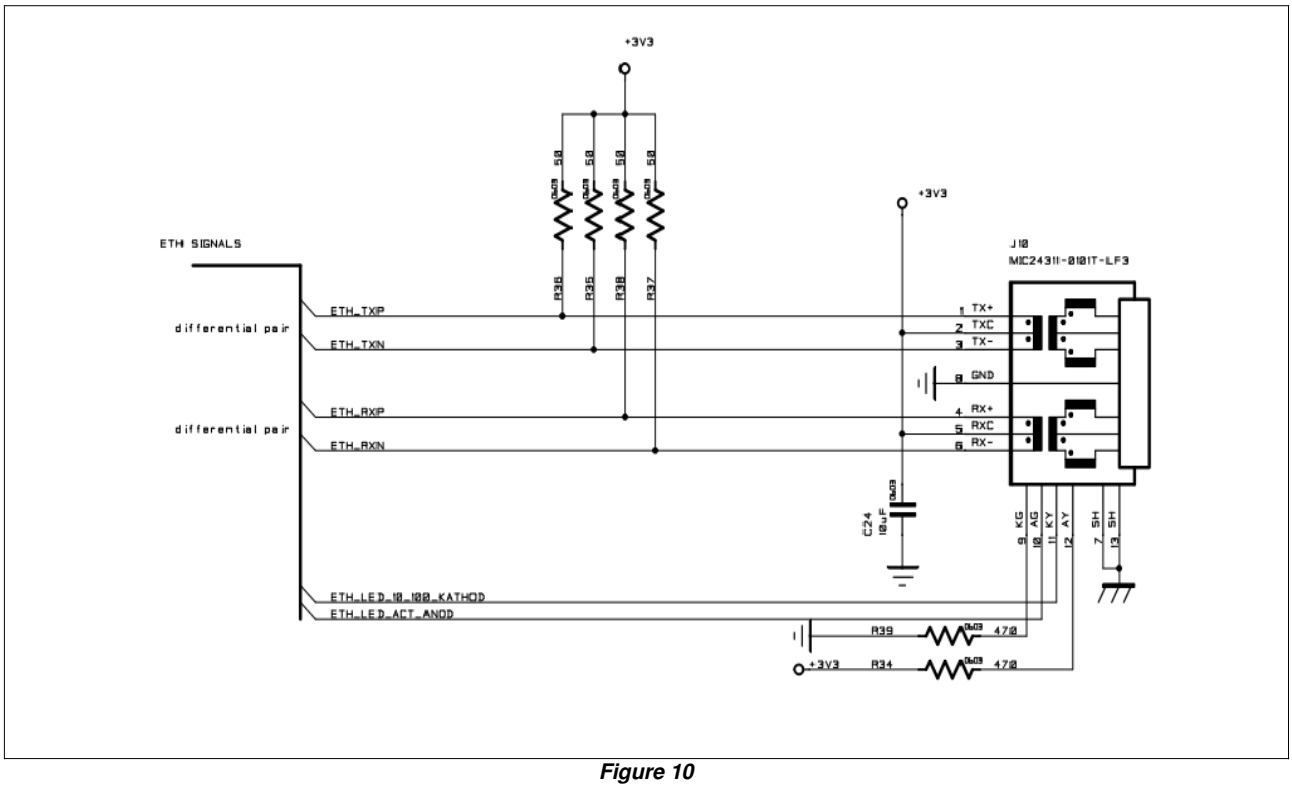


Figure 10

Number	Name	Primary Function Description	GPIO Capable	Voltage
127	ETH_TXN	Fast Ethernet Controller TXN signal	-	+3,3V
129	ETH_TXP	Fast Ethernet Controller TXP signal	-	+3,3V
131	ETH_RXN	Fast Ethernet Controller RXN signal	-	+3,3V
133	ETH_RXP	Fast Ethernet Controller RXP signal	-	+3,3V
137*	ETH_LED_10_100_KATHOD	Led Indicator Kathod signal	-	+3,3V
139*	ETH_LED_ACT_ANOD	Led indicator Anod signal	-	+3,3V

Table 11

* If not used, this pin must be left floating.

Component Placement considerations

Components placement can affect signal quality, emissions and can decrease EMI problems.
If the magnetics are a discrete component than the distance from the connector RJ45 should be kept to under 25mm of separation.
To decrease EMI problems the distance between magnetics and Phy should be at least 25mm or greater.
The distance between Phy and RJ45 connector should always be within 200 mm.
The differential transmit pair should be keep at least 25mm from the edge of PCB up to the magnetics. If the magnetics are integrated into RJ45 the differential pair should be routed to the back of integrated magnetics RJ45 connector , away from the board of PCB.
The 49.9 ohm pull-up resistors on the differential lines should be placed within 10 mm of the Phy device
The signals RX & TX should be independently matched in length to within 6mm

How to connect the USB/OTG interface

The Freescale iMx25 USB module provides high performance USB On-The-Go (up to 480Mbps), compatible with the USB 2.0 specification. An OTG HS PHY is also integrated so no external OTG PHY is needed on GEA baseboard. In figure 11 is shown how the MINI-AB USB/OTG connector is powered and connected to the GEA module on the GEA Starter Kit. An external +3,3V to +6V power supply is sustained where host functionality are requested. In Table 12 are listed all USB/OTG signal of GEA module.

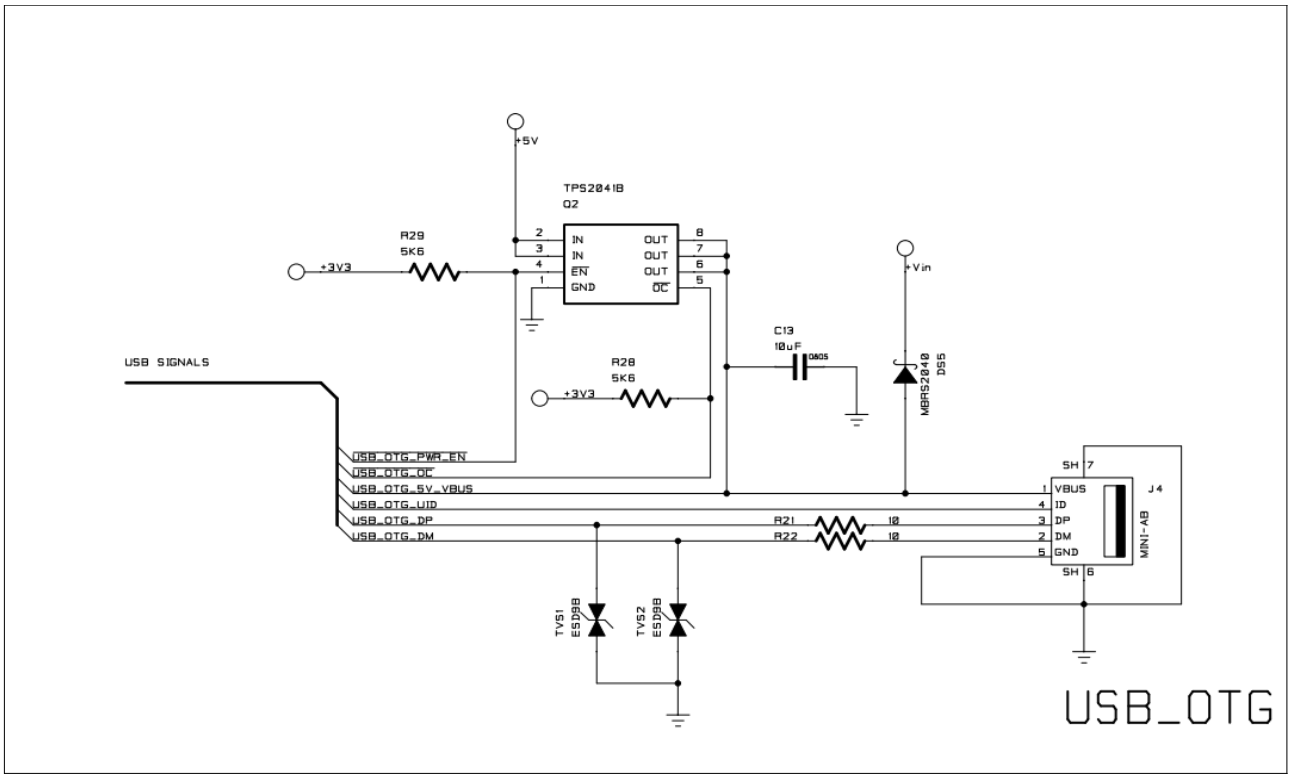


Figure 11

Number	Name	Primary Function Description	GPIO Capable	Voltage
195	USB_OTG_5V_VBUS	USB on the go interface	N	-
192	USB_OTG_DP	USB on the go interface	N	-
83 / 119	USB_OTG_OC#	USB on the go interface	Y	+1,8V
191	USB_OTG_UID	USB on the go interface	N	-
81 / 118	USB_OTG_PWR_EN#	USB on the go interface	Y	+1,8V
193	USB_OTG_DM	USB on the go interface	N	-

Table 12

How to connect the SD/CARD interface

The Freescale iMx25 enhanced Secured Digital Host Controller (eSDHC) provides the interface between the host system and MMC/SD/SDIO/CE-ATA cards, including cards with reduced size or mini cards. GEA module include this features and in figure 12 is shown how the MicroSD Card connector is connected to GEA Module on the GEA Starter Kit. The GEA Module eSDHC signal are listed in table 13.

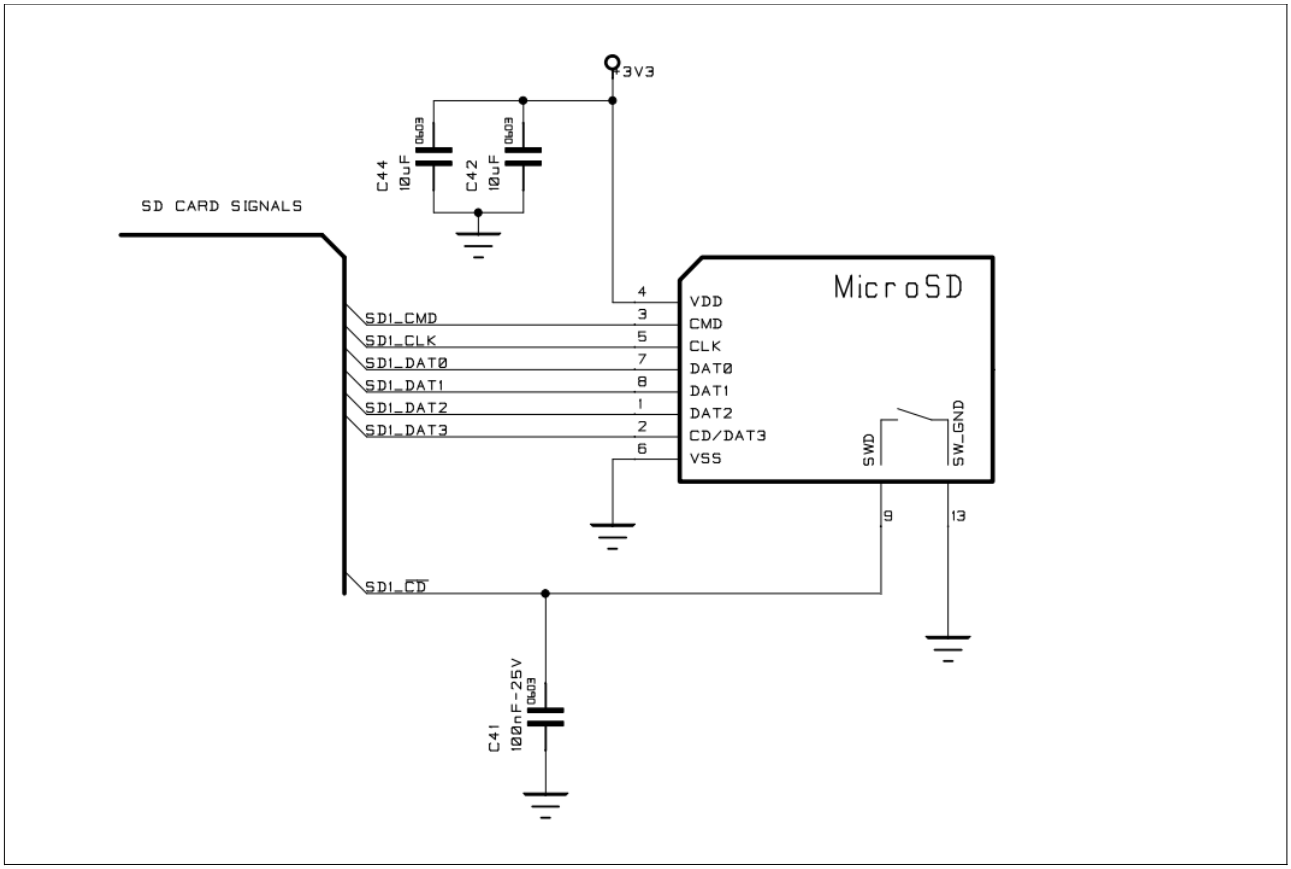


Figure 12

Number	Name	Primary Function Description	GPIO Capable	Voltage
183	SD1_CD#	eSDHC CD Signal	Y	+1,8V
184	SD1_WP	eSDHC WP Signal	Y	+1,8V
188	SD1_DAT0	eSDHC DAT 0 signal	Y	+3,3V
187	SD1_DAT1	eSDHC DAT 1 signal	Y	+3,3V
185	SD1_DAT2	eSDHC DAT 2 signal	Y	+3,3V
189	SD1_CLK	eSDHC CLK signal	Y	+3,3V
190	SD1_CMD	eSDHC CMDsignal	Y	+3,3V
186	SD1_DAT3	eSDHC DAT 3 signal	Y	+3,3V

Table 13

How to connect a LCD display

The Freescale iMx25 LCD controller (LCDC) provides display data for external greyscale or color LCD panels. LCDC is capable of supporting black-and-white, greyscale, passive-matrix color (passive color or CSTN), and active-matrix color (active color or TFT) LCD panels. The maximum supported resolution is 800x600. GEA Starter Kit is equipped with a 3.5" LCD wit a 320x240 resolution. In figure 13 is shown how the LCD 40 pin connector is connected to the GEA module. In Table 14 are listed all LCDC signals of GEA Module. Please refer to iMx25 reference manual for further details.

Number	Name	Primary Function Description	GPIO Capable	Voltage
143	LCD_D15	LCD interface	N	+3,3V
132	LCD_CONTRAST	LCD interface	Y	+3,3V
145	LCD_D13	LCD interface	N	+3,3V
162	LCD_OE	LCD interface	Y	+3,3V
148	LCD_D10	LCD interface	N	+3,3V
144	LCD_D14	LCD interface	N	+3,3V
152	LCD_D6	LCD interface	Y	+3,3V
154	LCD_D4	LCD interface	Y	+3,3V
147	LCD_D11	LCD interface	N	+3,3V
125	LCD_LSCLK_PCLK_FPSHIFT	LCD interface	Y	+3,3V
151	LCD_D7	LCD interface	Y	+3,3V
159	LCD_D0	LCD interface	Y	+3,3V
149	LCD_D9	LCD interface	N	+3,3V
146	LCD_D12	LCD interface	N	+3,3V
157	LCD_D2	LCD interface	Y	+3,3V
160	LCD_VSYNC	LCD interface	Y	+3,3V
161	LCD_HSYNC	LCD interface	Y	+3,3V
150	LCD_D8	LCD interface	N	+3,3V
153	LCD_D5	LCD interface	Y	+3,3V
155	LCD_D3	LCD interface	Y	+3,3V
158	LCD_D1	LCD interface	Y	+3,3V
141	LCD_D17	LCD interface	Y	+3,3V
142	LCD_D16	LCD interface	Y	+3,3V

Table 14

Connection map for 18 bit TFT only

The following map rappresent the connection mode applied to 18 bit TFT display
For every connection the color controlled is joined

Number	Name	18 bit TFT connections
159	LCD_D0	BLU 0
158	LCD_D1	BLU 1
157	LCD_D2	BLU 2
155	LCD_D3	BLU 3
154	LCD_D4	BLU 4
153	LCD_D5	BLU 5
152	LCD_D6	GREEN 0
151	LCD_D7	GREEN 1
150	LCD_D8	GREEN 2
149	LCD_D9	GREEN 3
148	LCD_D10	GREEN 4
147	LCD_D11	GREEN 5
146	LCD_D12	RED 0
145	LCD_D13	RED 1
144	LCD_D14	RED 2
143	LCD_D15	RED 3
142	LCD_D16	RED 4
141	LCD_D17	RED 5

Table 14a

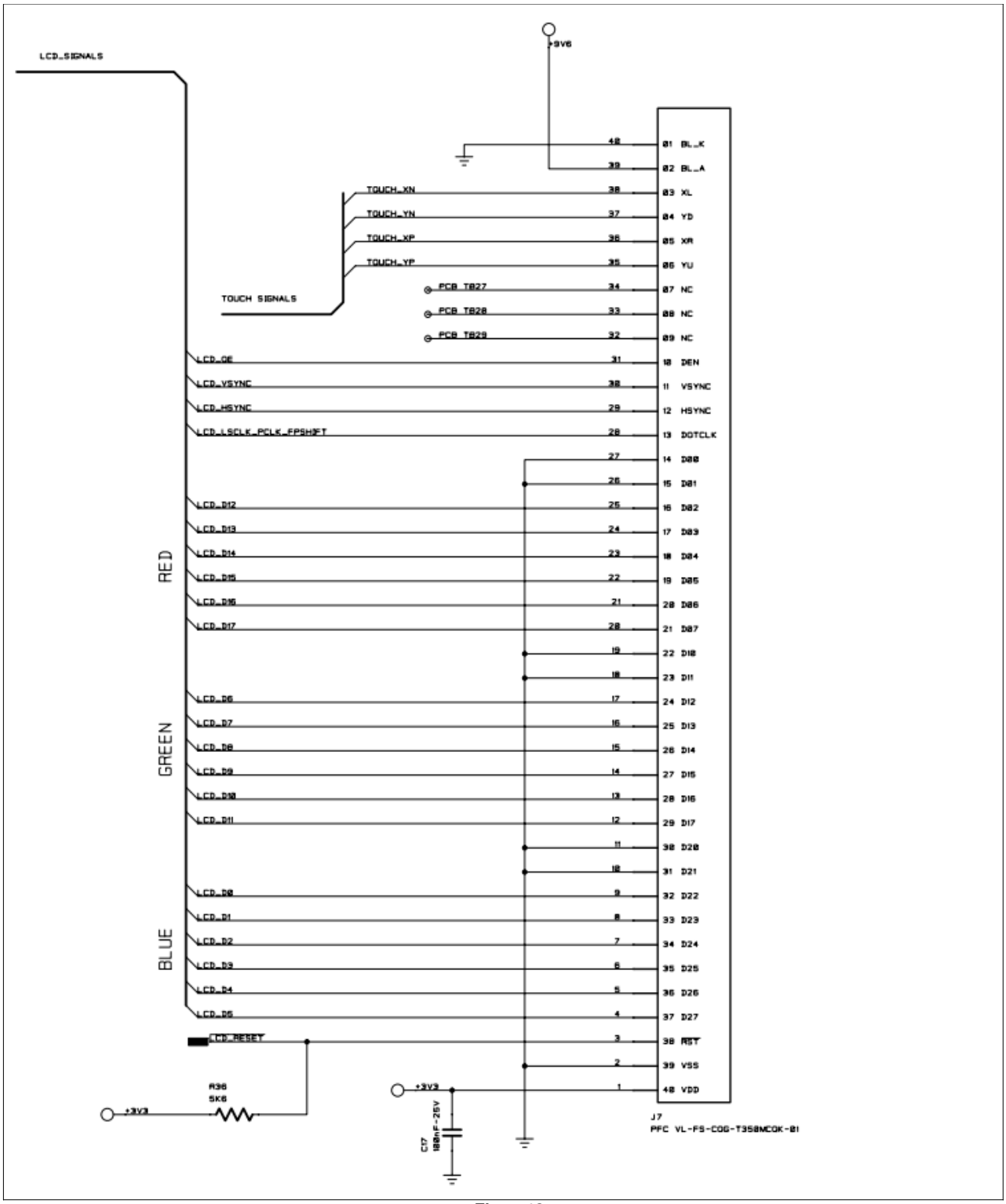

LCD_SIGNALS
+5V6
TOUCH_XN
TOUCH_YN
TOUCH_XP
TOUCH_YP
PCB_TP27
PCB_TP28
PCB_TP29
TOUCH SIGNALS
LCD_OE
LCD_VSYNC
LCD_HSYNC
LCD_LSCLK_PCLK_FPSHIFT
RED
GREEN
BLUE
LCD_RESET
R36
5K6
+3V3
C17
100nF-25V
J7
PFC VL-FS-COG-T35BMCOK-01
01 BL_K
02 BL_A
03 XL
04 YD
05 XR
06 YU
07 NC
08 NC
09 NC
10 DEN
11 VSYNC
12 HSYNC
13 DOTCLK
14 D00
15 D01
16 D02
17 D03
18 D04
19 D05
20 D06
21 D07
22 D10
23 D11
24 D12
25 D13
26 D14
27 D15
28 D16
29 D17
30 D20
31 D21
32 D22
33 D23
34 D24
35 D25
36 D26
37 D27
38 RST
39 VSS
40 VDD

Figure13

How to connect the USB host interface

Figure 14 is shown how to connect the USB host interface to GEA Module. An external +3,6V to +6V range power supply is sustained where host functionality are requested. In Table 15 are listed all USB Host interface signal of GEA module.

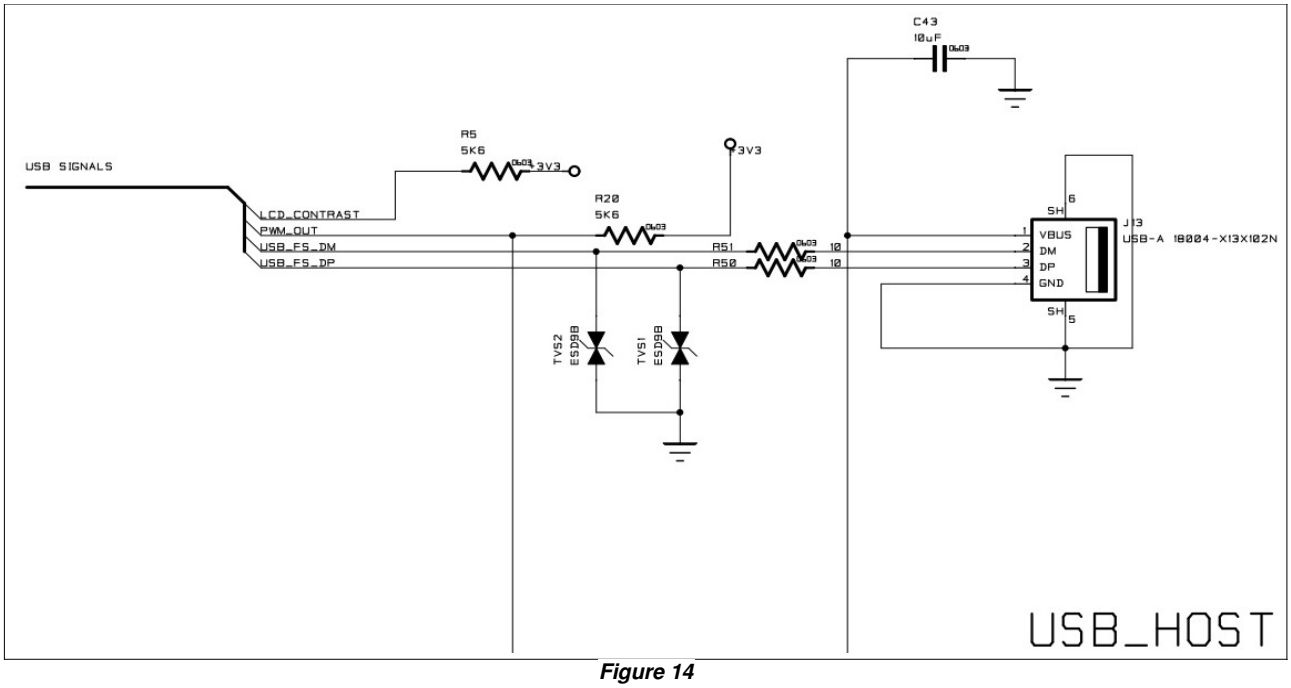


Figure 14

Number	Name	Primary Function Description	GPIO Capable	Voltage
94	PWM_OUT	PWM Out signal	Y	+1,8V
132	LCD_CONTRAST	LCD interface	N	+3,3V
194	USB_FS_DP	USB HOST interface	N	-
196	USB_FS_DM	USB HOST interface	N	-

Table 15

JTAG Interface

Joint Test Action Group (**JTAG**) is the common name used for the IEEE 1149.1 standard entitled **Standard Test Access Port and Boundary-Scan Architecture** for test access ports used for testing printed circuit boards using boundary scan. JTAG is often used as an IC debug or probing port.

There are no official standards for JTAG adapter physical connectors. Development boards usually include a header to support preferred development tools; in some cases they include multiple such headers, because they need to support multiple such tools. For example, a microcontroller, FPGA, and ARM application processor will rarely share tools, so a development board using all of those components might have three or more headers. Production boards may omit the headers; or when space is tight, just provide JTAG signal access using test points.

Figure 15 is shown how to connect a JTAG interface to GEA Module. In Table 16 are listed all JTAG signals of GEA Module. Please refer to iMx25 reference manual for further details.

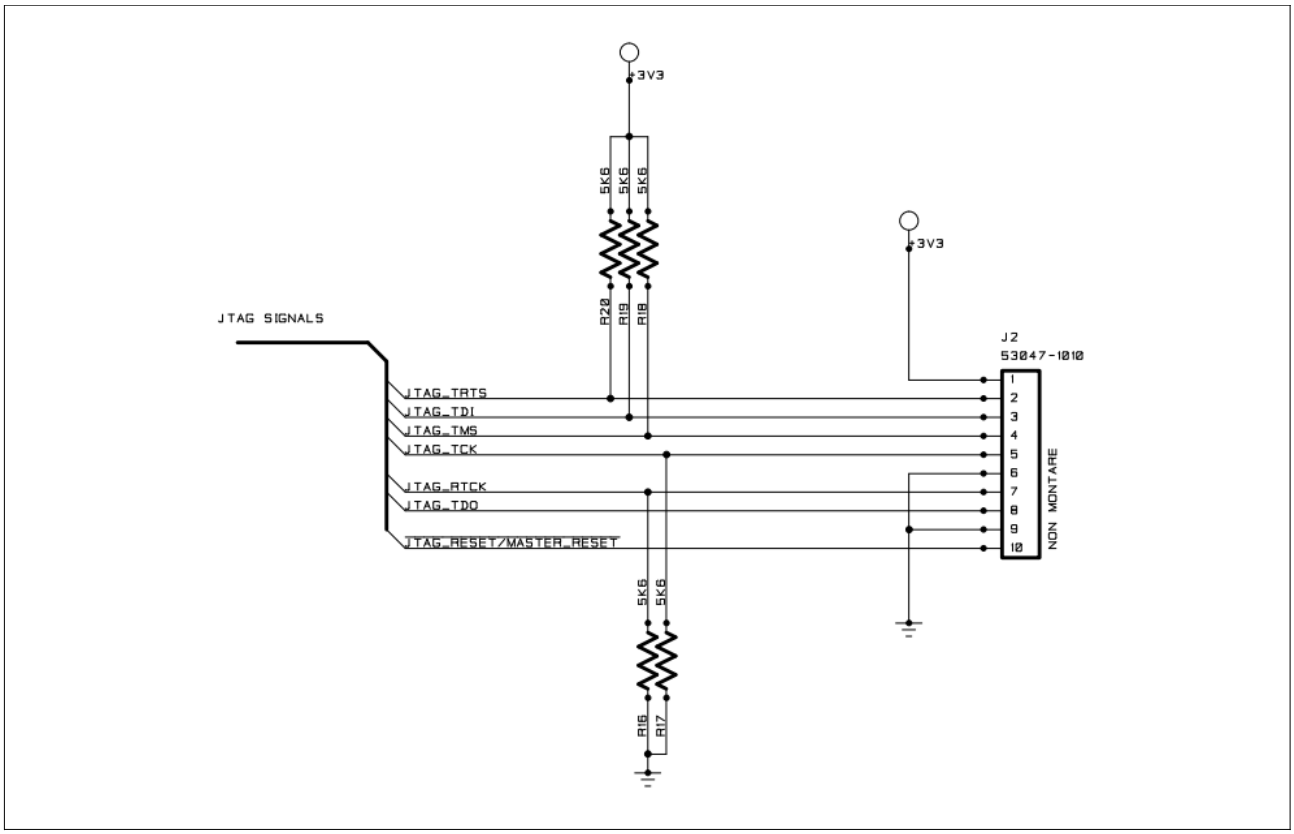


Figure 15

Number	Name	Primary Function Description	GPIO Capable	Voltage
172	JTAG_DE	JTAG Interface	N	-
174	JTAG_TD0	JTAG Interface	N	-
175	JTAG_TDI	JTAG Interface	N	-
178	JTAG_RTCK	JTAG Interface	N	-
177	JTAG_TCK	JTAG Interface	N	-
179	JTAG_RESET/MASTER_RESET#	JTAG Interface	N	-
173	JTAG_TRTS	JTAG Interface	N	-
176	JTAG_TMS	JTAG Interface	N	-

Table 16

NB: The JTAG_DE signal is not routed on the evaluation board

Boot Mode Pin

Boot mode pin determines how GEA module boot. The possible options are listed in Table 17:

BOOT_MODE	Action
0	Boot from internal flash
1	Boot from USB/OTG

Table 17

The boot from USB OTG usually is used for the bootloader deploy.

Figure 16 is shown the boot section of GEA started kit. Closing JM1 correspond to put at logical 1 the bootmode pin.

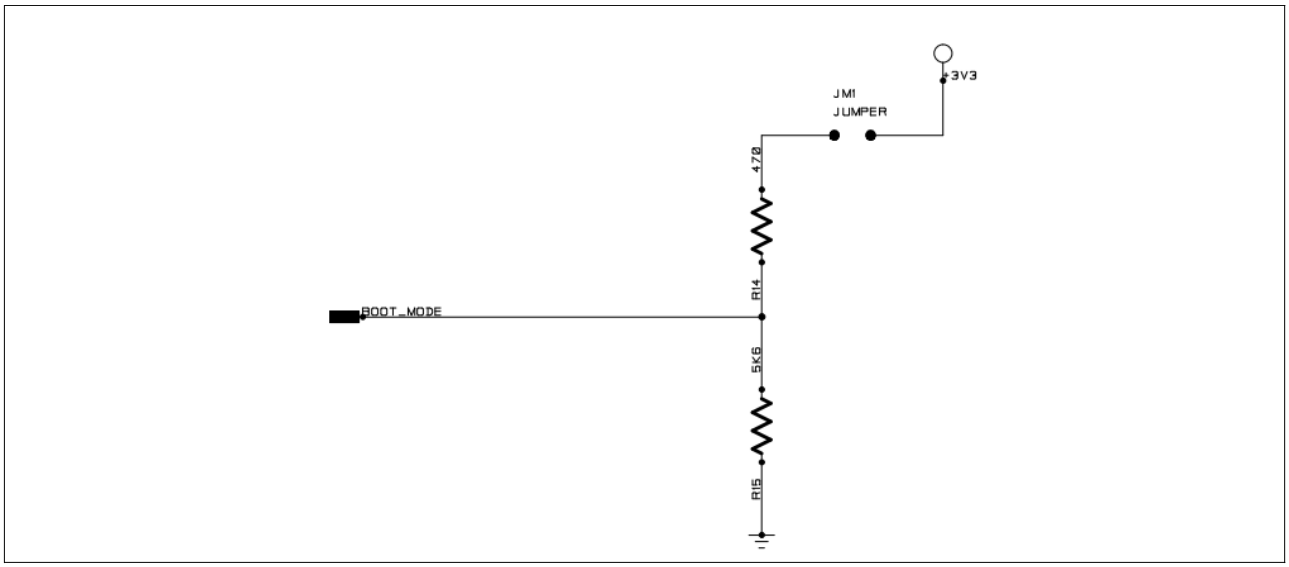


Figure 16

In Table 18 is listed the boot mode Pin numbering.

Number	Name	Primary Function Description	GPIO Capable	Voltage
181	BOOT_MODE	Boot from USB/Uart or on board Nand Flash	Y	-

Table 18

Peripheral multiplexing description

Following we describe opportunity to use alternative interfaces using the properties of multiplexing pin

SPI & IIS Configuration

Using pin multiplexing's features we may have the following SPI and IIS connections. In the tables below are shown the output signals on the Connector's module.

SPI1 signals interfaces

Pin number	Signal reference	Voltage reference
167	MOSI	+3,3V
168	MISO	+3,3V
169	SCK	+3,3V
171	SS0	+3,3V
170	SS1	+3,3V

Table 19

SPI2 signals interfaces

Pin number	Signal reference	Voltage reference
146	MOSI	+3,3V
145	MISO	+3,3V
144	SCK	+3,3V
162	SS0	+3,3V
132	SS1	+3,3V

Table 20

SPI3 signals interfaces

Pin number	Signal reference	Voltage reference
6	MOSI	+3,3V
7	MISO	+3,3V
8	SCK	+3,3V
10	SS0	+3,3V
11	SS1	+3,3V

Table 21

SPI4 signals interfaces

Pin number	Signal reference	Voltage reference
61	MOSI	+1,8V
60	MISO	+1,8V
67	SCK	+1,8V
65	SS0	+1,8V
55	SS1	+1,8V

Table 22

The following tables show the pin configurations for IIS Bus on module's connector.

IIS1 bus interfaces

Pin number	Signal reference	Voltage reference
65	I2S_DIN	+1,8V
55	I2S_DOUT	+1,8V
70	I2S_SCLK	+1,8V
61	I2S_MCLK	+1,8V
57	I2S_LRCLK	+1,8V

Table 23

IIS2 bus interfaces

Pin number	Signal reference	Voltage reference
104	I2S_DIN	+3,3V
103	I2S_DOUT	+3,3V
102	I2S_SCLK	+3,3V
106	I2S_MCLK	+3,3V
101	I2S_LRCLK	+3,3V

Table 24

IIS3 bus interfaces

Pin number	Signal reference	Voltage reference
17	I2S_DIN	+3,3V
14	I2S_DOUT	+3,3V
15	I2S_SCLK	+3,3V
12	I2S_MCLK	+3,3V
16	I2S_LRCLK	+3,3V

Table 25

Alternative PWM pins table

It's possible to set the pins shown in the following table as PWM signals.

Pin number	Signal reference	Voltage reference
94	PWM1	+3,3V
118 alternative pin 171	PWM2	+3,3V
119	Pwm3	+3,3V
120 alternative pin 132	PWM4	+3,3V

Table 26

General Purpose Timer (GPT) & IIC Configuration

Using pin multiplexing's features we may have the following GPT and IIC connections. In the tables below are shown the output signals on the Connector's module.

GPT1 interfaces

Pin number	Signal reference	Voltage reference
120	CAPIN1	+3,3V
121	CMPOUT1	+3,3V

Table 27

GPT2 interfaces

Pin number	Signal reference	Voltage reference
111	CAPIN1	+3,3V
110	CMPOUT1	+3,3V

Table 28

GPT3 interfaces

Pin number	Signal reference	Voltage reference
115	CAPIN1	+3,3V
114	CMPOUT1	+3,3V

Table 29

GPT4 interfaces

Pin number	Signal reference	Voltage reference
132	CAPIN1	+3,3V
94	CMPOUT1	+3,3V

Table 30

IIC Configuration

IIC1 interfaces

Pin number	Signal reference	Voltage reference
23	SCL	+3,3V
24	SDA	+3,3V

Table 31

IIC2 interfaces

Pin number	Signal reference	Voltage reference
120	SCL	+3,3V
121	SDA	+3,3V

Table 32

IIC3 interfaces

Pin number	Signal reference	Voltage reference
118 alternative pin 160	SCL	+3,3V
119 alternative pin 170	SDA	+3,3V

Table 33

Alternative UART pins table

The following table shows an alternative UART configuration +3,3 and +1,8 volts compliant

UART1 interfaces

Pin number	Signal reference	Voltage reference
114	UART1_CTS	+3,3V
115	UART1_RTS	+3,3V
116	UART1_TXD	+3,3V
117	UART1_RXD	+3,3V

Table 34

UART2 interfaces

Pin number	Signal reference	Voltage reference
110	UART2_CTS	+3,3V
111	UART2_RTS	+3,3V
112	UART2_TXD	+3,3V
113	UART2_RXD	+3,3V

Table 35

UART3 interfaces

Pin number	Signal reference	Voltage reference
105 alternative pin 169	UART3_CTS	+3,3V
106 alternative pin 170	UART3_RTS	+3,3V
108 alternative pin 168	UART3_TXD	+3,3V
109 alternative pin 167	UART3_RXD	+3,3V

Table 36

UART4 interfaces

Pin number	Signal reference	Voltage reference
101	'UART4_CTS'	+3,3V
102	UART4_RTS	+3,3V
103	UART4_TXD	+3,3V
104	UART4_RXD	+3,3V

Table 37

UART5 interfaces

Pin number	Signal reference	Voltage reference
9 alternative pin 61	UART5_CTS	+3,3V alternative +1,8V
8 alternative pin 60	UART5_RTS	+3,3V alternative +1,8V
7 alternative pin 67	UART5_TXD_MUX	+3,3V alternative +1,8V
6 alternative pin 69	UART5_RXD_MUX	+3,3V alternative +1,8V

Table 38