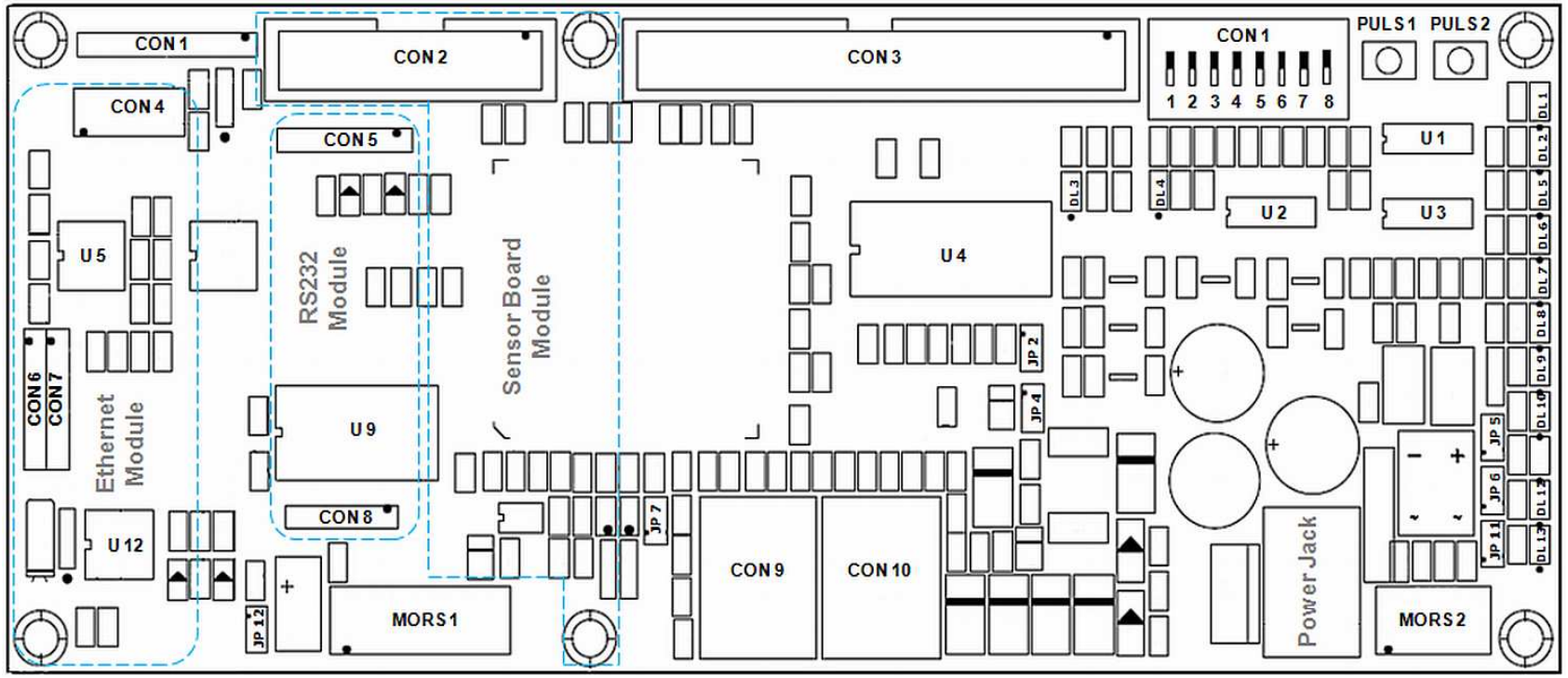

Figure 1: FPGA

Push Btns.	pos. 1-2 (normal)	pos. 3-4 (pressed)
PULS 1	U2 (DS)	GND
PULS 2	+3.3V	GND

Power Supply Connector [MORS 2]	
Pin 1	VAC 1
Pin 2	VAC 2
Pin 3	EARTH

Note1: Input 9-36V DC
Note2: Connect either ‘MORS2’ or ‘Power Jack’. NEVER connect both!

ZigBee Connector [CON 6 + CON 7]					
CON 6			**CON 7**		
Pin		FPGA	Pin		FPGA
1	+3.3V	-	1	GND	-
2	SS	87	2	INT2	77
3	CN1	76	3	INT1	75
4	SDO_ETH	85	4	SDI_ETH	106
5	SCK_ETH	10	5	CCA	84
6	GP1	86	6	FIFOP	82

LEDs		
		FPGA
DL 1 (red)	U1 (Q7)	-
DL 2 (red)	U1 (Q6)	-
DL 3 (yellow)	-	122
DL 4 (yellow)	U3 (Q0)	-
DL 5 (red)	U1 (Q5)	-
DL 6 (red)	U1 (Q4)	-
DL 7 (red)	U1 (Q3)	-
DL 8 (red)	U1 (Q2)	-
DL 9 (red)	U1 (Q1)	-
DL 10 (red)	U1 (Q0)	-
DL 12 (green)	Power +3.3V	-
DL 13 (green)	Power +5V	-

DIP Switches [DP1]			
No.	**Pin**	**OFF**	**ON**
1	D7	U2 (DS)	GND
2	D6	U2 (DS)	GND
3	D5	U2 (DS)	GND
4	D4	U2 (DS)	GND
5	D3	U2 (DS)	GND
6	D2	U2 (DS)	GND
7	D1	U2 (DS)	GND
8	D0	U2 (DS)	GND

Note: Default positions are indicated with grey background

JTAG Connector [CON 1]		
Pin		FPGA
1	VDD (+3.3V)	-
2	TDO	129
3	TDI	128
-	-	-
5	TMS	126
6	GND	-
7	TCK	127

RS232 Slot [CON 5]		
Pin		FPGA
1	+5V	-
2	TX	163
3	RTS	114
4	RX	164
5	CTS	113
6	GND	-

RS232 Slot (PC Side) [CON 8]	
Pin 1	CTS
Pin 2	RX
Pin 3	TX
Pin 4	RTS
Pin 5	GND

UART Connector (PC Side) [MORS 1]	
Pin 1	GND
Pin 2	CTS
Pin 3	RX
Pin 4	RTS
Pin 5	TX

Sensor Board Connector [CON 2]					
Pin		FPGA	Pin		FPGA
1	GND	-	2	VCC_CAM	-
3	C0	139	4	C15	140
5	C1	146	6	C14	147
7	C2	150	8	C13	151
9	C3	142	10	C12	145
11	C4	148	12	C11	149
13	C5	156	14	C10	155
15	C6	157	16	C9	158
17	C7	159	18	C8	160
19	-	-	20	+5V	-

Jumper	open	close
JP 2	SDRAM (+3.3V) power regulated by FPGA	SDRAM always powered on
JP 4	ASRAM (+3.3V) power regulated by FPGA	ASRAM always powered on
JP 5	*UNUSED*	
JP 6	LED (+3.3V) OFF	LED (+3.3V) ON
JP 7	*ALWAYS LEAVE OPEN*	
JP 11	LED (+5V) OFF	LED (+5V) ON
JP 12	CHARGING OFF	CHARGE BATTERY (RTC)

Note: Default jumper settings are indicated with grey background

LCD Display Connector [CON 3]

Pin		FPGA	Pin		FPGA
1	+5V	-	2	+3.3V	-
3	GND	-	4	GND	-
5	VDD_LCD	-	6	VDD_LCD	-
7	CONF_LCD	144	8	RST_LCD	105
9	CS_LCD	111	10	D/C_LCD	110
11	E(RD)_LCD	116	12	R/W_LCD	115
13	D0	167	14	D1	168
15	D2	169	16	D3	170
17	D4	173	18	D5	174
19	D6	175	20	D7	176
21	D8	120	22	D9	118
23	D10	132	24	D11	121
25	D12	137	26	D13	135
27	D14	138	28	D15	136
29	INT_SDA	41	30	INT_SCL	40
31	FREE_LCD	97	32	VDD_LCD	-
33	VDD_LCD	-	34	GND	-
35	SDO_PIC32	112	36	CLS_LCD	123
37	SDI_PIC32	45	38	BUSY_LCD	124
39	SCK_PIC32	51	40	PENIRQL_LCD	125

Ethernet Connector [CON 4]

Pin		FPGA	Pin		FPGA
1	SDO_ETH	85	2	SCK_ETH	103
3	SDI_ETH	106	4	GP1	86
5	SS	87	6	INT2	77
7	CN1	76	8	INT1	75
9	GND	-	10	+3.3V	-

RJ6 Motor Connector [CON 9]

Pin		FPGA
1	GND	-
2	CS_SPI_MOTOR	39
3	SCK_PIC32	51
4	SDI_PIC32	45
5	SDO_PIC32	112
6	+3.3V_OUT	-

RJ6 PIC32 Connector [CON 10]

Pin		FPGA
1	GND	-
2	CS_SPI_PIC32	52
3	SCK_PIC32	51
4	SDI_PIC32	45
5	SDO_PIC32	112
6	+3.3V_OUT	-

Output Multiplexer (SI – PO) [U 1]		
Pin		FPGA
1	LED DL9	-
2	LED DL8	-
3	LED DL7	-
4	LED DL6	-
5	LED DL5	-
6	LED DL2	-
7	LED DL1	-
11	CLK_HC	56
12	STR_HC	54
13	#OUT_EN_74HC595	55
14	OUT_HC	53
15	LED DL10	-

Input Multiplexer (PI – SO) [U 2]		
Pin		FPGA
1	STR_HC	54
2	CLK_HC	56
3	DP1 pin4	-
4	DP1 pin3	-
5	DP1 pin2	-
6	DP1 pin1	-
7	IN_HC	47
10	PULS1	-
11	DP1 pin8	-
12	DP1 pin7	-
13	DP1 pin6	-
14	DP1 pin5	-

SPI Flash [U 5]		
Pin		FPGA
1	SPI_CE	13
2	SPI_DI	20
5	SPI_DO	19
6	SPI_CL	17

Real Time Clock [U 12]		
Pin		FPGA
3	A0 - GND	-
5	INT_SDA	41
6	INT_SCL	40

SRAM [U 9]		
Pin		FPGA
1	A_SRAM4	206
2	A_SRAM3	207
3	A_SRAM2	8
4	A_SRAM1	7
5	A_SRAM0	6
6	CE#_SRAM	1
7	DQ1	2
8	DQ2	23
9	DQ3	21
10	DQ4	18
13	DQ5	12
14	DQ6	11
15	DQ7	10
16	DQ8	9
17	WE#_SRAM	30
18	A_SRAM15	31
19	A_SRAM14	32
20	A_SRAM13	33
21	A_SRAM12	34
22	A_SRAM16	35

SRAM [U 9]		
Pin		FPGA
23	A_SRAM17	201
24	A_SRAM11	202
25	A_SRAM10	36
26	A_SRAM9	44
27	A_SRAM8	205
28	A_SRAM18	15
29	DQ9	198
30	DQ10	197
31	DQ11	196
32	DQ12	195
35	DQ13	194
36	DQ14	193
37	DQ15	192
38	DQ16	189
39	CB_SRAM	43
40	OB_SRAM	42
41	OE#_SRAM	188
42	A_SRAM7	187
43	A_SRAM6	186
44	A_SRAM5	185

SDRAM [U 4]		
Pin		FPGA
2	D0	167
4	D1	168
5	D2	169
7	D3	170
8	D4	173
10	D5	174
11	D6	175
13	D7	176
15	A15	73
16	SDWE#	72
17	CAS#_SDRAM	68
18	RAS#_SDRAM	67
19	#CS_DRAM	69
20	A13	66
21	A14	65
22	A10	64
23	A0	63
24	A1	60
25	A2	59

SDRAM [U 4]		
Pin		FPGA
26	A3	74
29	A4	78
30	A5	83
31	A6	88
32	A7	92
33	A8	94
34	A9	98
35	A11	91
36	A12	93
37	CKE_DRAM	101
38	SDCK_DRAM	102
39	CFIOW_NBS3_NWR	104
42	D8	120
44	D9	118
45	D10	13
47	D11	121
48	D12	137
50	D13	135
51	D14	138
53	D15	136

Output Multiplexer (SI – PO) [U 3]		
Pin		FPGA
1	C_VCC_SRAM	-
2	C_VCC_LCD	-
3	C_VCC_FLASH	-
4	C_VCC_DRAM	-
5	C_VCC_CAM	-
6	VCC_DIP_SWITCH	-
7	C_3.3V_OUT	-
11	CLK_HC	56
12	STR_HC	54
13	#OUT_EN_74HC595	55
15	LED DL4	-